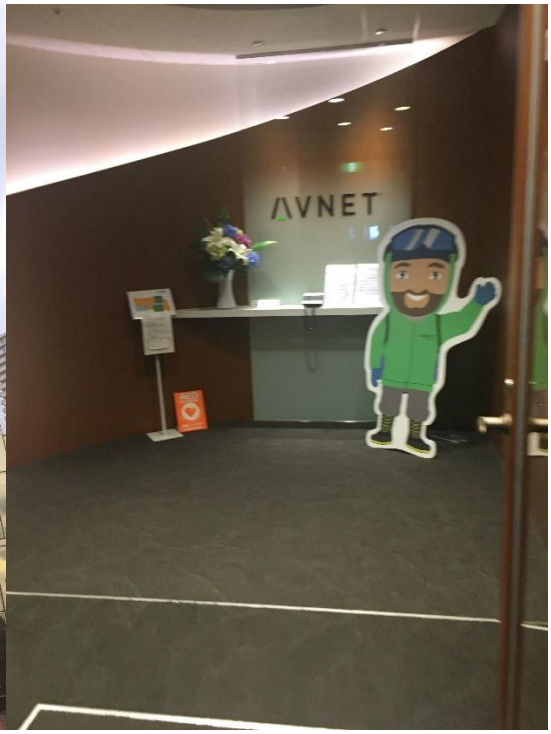
XILINX University Program Workshop Participation Report

群馬大学大学院 理工学府 電子情報・数理教育プログラム 博士 1 年 孫逸菲

Data and Time : 2017 年４月２６日　　１０：００～１７：３０
Course：Using Vivado Design Suite　Artix-7 FPGA design and development
Place: アヴネット株式会社 東京本社 Training Room

This time I participate in using Vivado design suite to design and development of Artix-7 FPGA. Place is the 23 floor of the Ebisu Garden Place Tower.

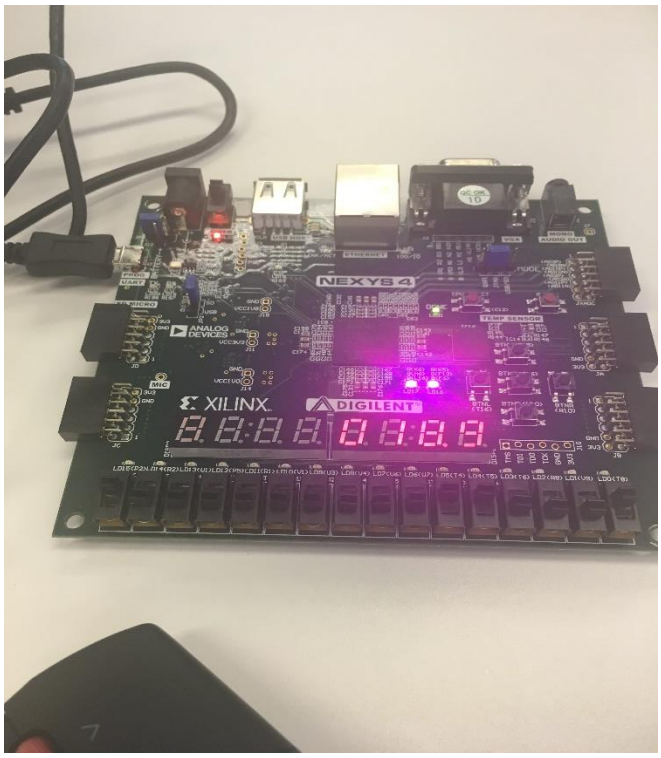
Ebisu Garden Place Tower



Avnet Co., Ltd. Tokyo Head Office

Six people attended the course, the company has prepared the computer, Artix-7 product description and Nexys 4 Artix-7 FPGA trainer board for each of us. At morning the lecturer introduces the basic knowledge of Artix-7 FPGA. And on the afternoon, The main is conducted the exercise of Nexys4&Vivado tool flow. Follow the steps below: At first create a new project, the second is adding a design file to a project. Than create IP from IP catalog (generate memory and PLL). Than execution of RTL analysis and logic synthesis. After, XDC creation and set the time. At the end, implementation and generate bit stream, download to ARTY with hardware manager. Artix-7 devices providing the highest performance to power

ratio structure in a single cost optimized FPGA. This series provides maximum value for all types of cost-sensitive applications. Including software defined radio, machine vision photography and low-end wireless return.



Nexys 4 Artix-7 FPGA trainer board

Before I have used of ISE software to simulation in RTL level, have not used Vivado software. This time I have a comprehensive understanding of the software, to download the design, we use Nexys4.